Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (previously presented) A semiconductor package device comprising:

a semiconductor chip including a plurality of bonding pads having a microscopic size and aligned at a minute interval;

a first planar layer formed on the semiconductor chip ;

a second planar layer formed on the first planar layer;

an oxide layer made of polyimide based material formed on the second planar layer, wherein the bonding pads are exposed through openings in the first planar layer, the second planar layer, and the oxide layer;

a seed metal layer formed on the oxide layer, on the first and second planar layers exposed in the openings, and on the bonding pads exposed through the openings;

metal patterns formed on the seed metal layer,

wherein each metal pattern is electrically connected to one of the bonding pads,

wherein the area of each metal pattern on the oxide layer is larger than the area of the bonding pad to which the metal pattern is electrically connected, and

wherein the oxide layer relieves stress on each bonding pad

applied through the electrically connected metal pattern.

2. (cancelled) .

3. (original) The semiconductor package device as claimed in claim 1, wherein a total thickness of the metal patterns and the seed metal layer is about 1 to 10μm.

4. (original) The semiconductor package device as claimed in claim 1, wherein the seed metal layer has a triple stack structure including Ti-NiV-CU layers.

5. (original) The semiconductor package device as claimed in claim 1, wherein the bonding pads have a size of 10x10/μm in width and length.

6. (original) The semiconductor package device as claimed in claim 1, wherein the metal patterns include an Al-Ag alloy or a Cu-Ag alloy.

7. (original) The semiconductor package device as claimed in claim 1, wherein the metal patterns are aligned in left and right directions or upward and downward directions about the bonding pads.

8. (original) The semiconductor package device as claimed in claim 1, wherein the metal patterns are alternately aligned one by one in a zigzag manner in left and right directions or upward and downward directions about the bonding pads.

9. (previously presented) The semiconductor package device as claimed in claim 1 , wherein the metal patterns are inclined with a predetermined angle.

10. (previously presented) A semiconductor package device comprising:

a semiconductor chip including a plurality of bonding pads having a microscopic size and aligned at a minute interval;

a first planar layer formed on the semiconductor chip ;

a second planar layer formed on the first planar layer;

an oxide layer made of polyimide based material formed on the second planar layer, wherein the bonding pads are exposed through openings in the first planar layer, the second planar layer, and the oxide layer;

a seed metal layer formed on the oxide layer, on the first and second planar layers exposed in the openings, and on the bonding pads exposed through the openings;

metal patterns formed on the seed metal layer,

wherein each metal pattern is electrically connected to one of the bonding pads,

wherein the area of each metal pattern on the oxide layer is larger than the area of the bonding pad to which the metal pattern is electrically connected,

wherein the oxide layer relieves stress on each bonding pad applied through the electrically connected metal pattern, and

wherein the seed metal layer and the metal pattern is capable of being aligned in the left or right or up or down directions with respect to the electrically connected bonding pad.

11 (original) The semiconductor package device as claimed in claim 10, wherein the metal patterns include an Al-Ag alloy or a Cu-Ag alloy.

12. (original) The semiconductor package device as claimed in claim10, wherein the seed metal layer has a triple stack structure including Ti-NiV-CU layers.

13. (previously presented) A semiconductor package device comprising:

a semiconductor chip including a plurality of bonding pads having a

microscopic size and aligned at a minute interval;

a first planar layer formed on the semiconductor ;

a second planar layer formed on the first planar layer;

an oxide layer made of polyimide based material formed on the second planar layer, wherein the bonding pads are exposed through openings in the first planar layer, the second planar layer, and the oxide layer;

a seed metal layer formed on the oxide layer, on the first and second planar layers exposed in the openings, and on the bonding pads exposed through the openings;

metal patterns formed on the seed metal layer,

wherein each metal pattern is electrically connected to one of the bonding pads,

wherein the area of each metal pattern on the oxide layer is larger than the area of the bonding pad to which the metal pattern is electrically connected,

wherein the oxide layer relieves stress on each bonding pad applied through the electrically connected metal pattern, and

wherein the seed metal layer and metal patterns being alternately aligned one by one in a zigzag manner in left and right directions or upward and downward directions about the bonding pads.

14. (original) The semiconductor package device as claimed in claim 13, wherein the seed metal layer and metal patterns are alternately aligned while forming a slightly

inclined angle.

15-18. (cancelled)